

FIGURE 1. Typical 3G Receiver Functional Block Diagram, (Prior art)

TQ2070-000000000000

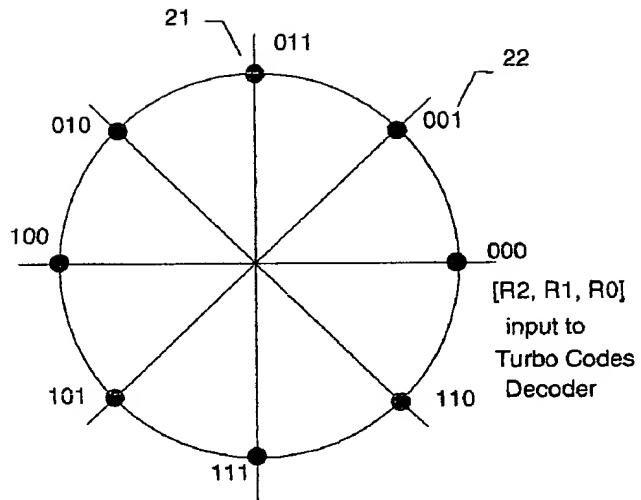
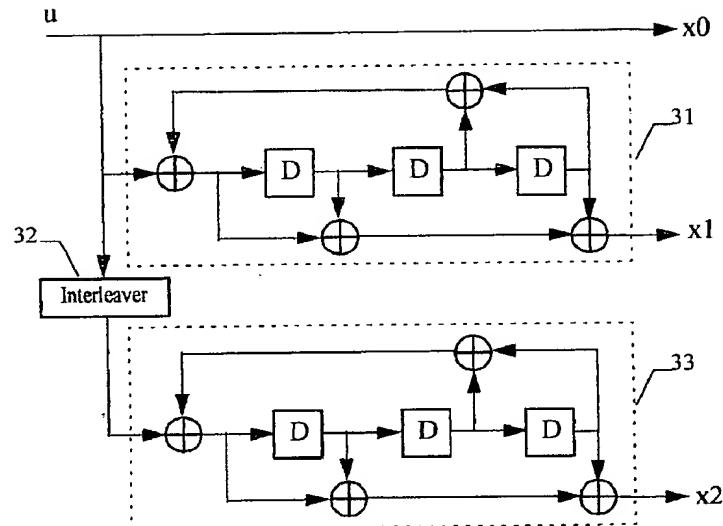


FIGURE 2. 8-PSK constellations, (Prior art)

10020000-2000100000



$$G(D) = [1, n(D) / d(D)]$$

$$\text{where, } d(D) = 1 + D2 + D3, n(D) = 1 + D + D3$$

FIGURE 3. The 8-states Parallel Concatenated Convolutional Code (PCCC),
(Prior art)

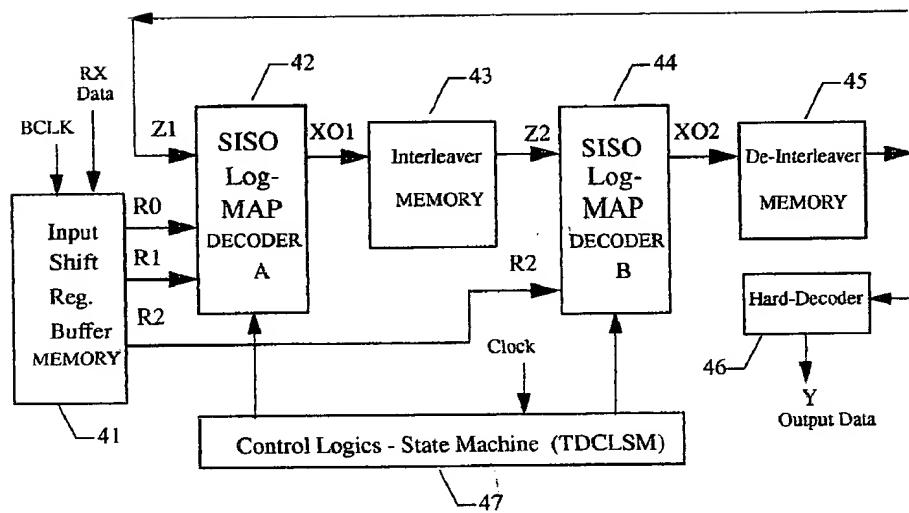


FIGURE 4. Turbo Codes Decoder System Block Diagram

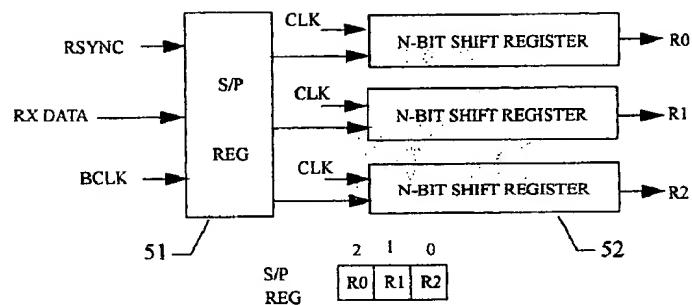


FIGURE 5. Input Buffer Shift Registers

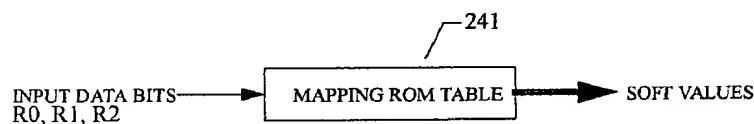


FIGURE 5b. Soft Values Mapping ROM Table

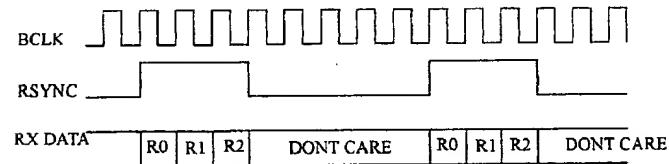


FIGURE 6. Input Buffer Interface Timing

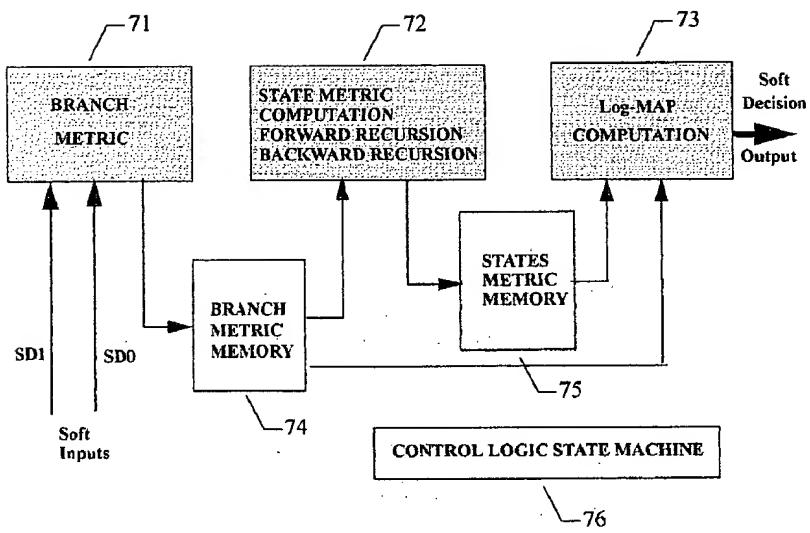


FIGURE 7. The 8-states SISO Log-MAP Decoder

00000000000000000000000000000000

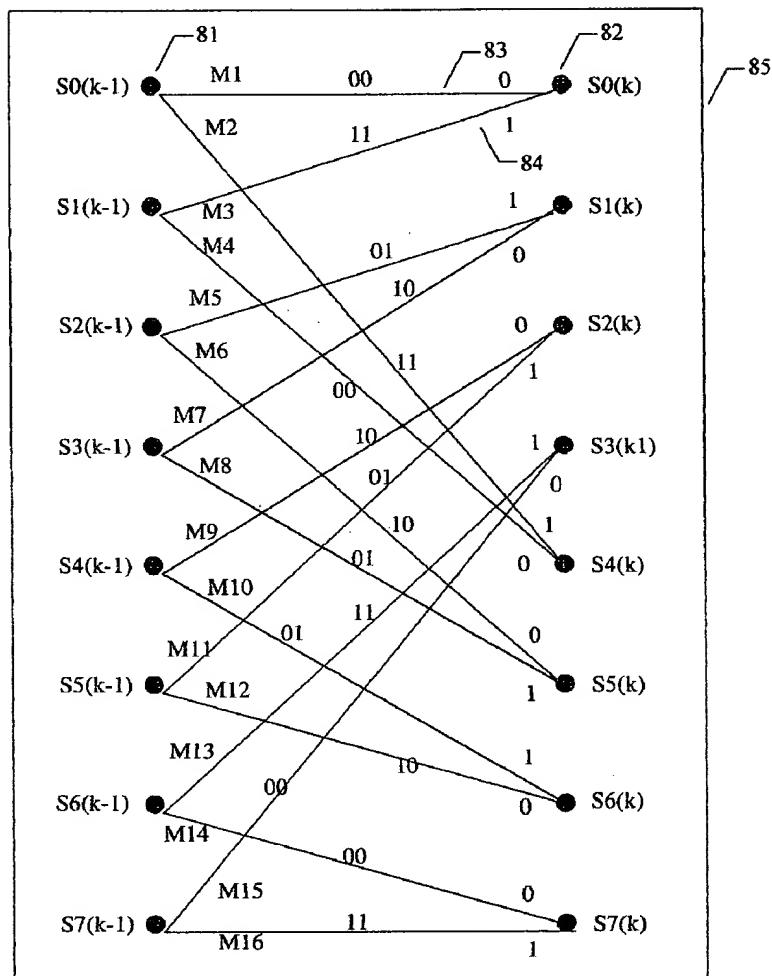


FIGURE 8. The 8-STATES TRELLIS DIAGRAM of a SISO Log-MAP Decoder

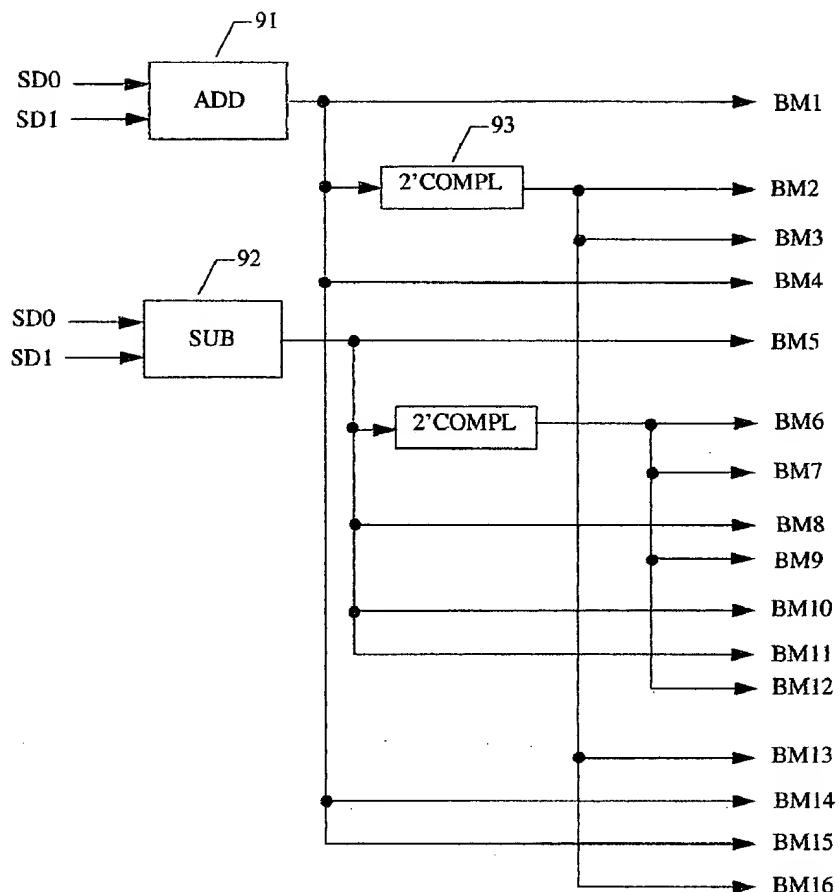


FIGURE 9. BRANCH METRIC COMPUTING MODULE

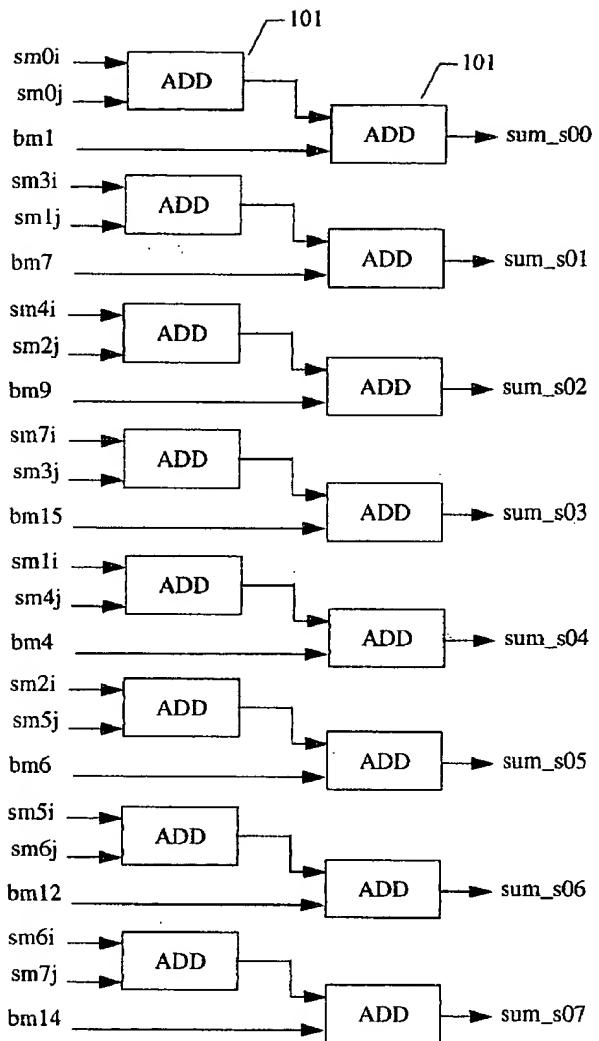


FIGURE 10a. LOG-MAP COMPUTING MODULE

T00070-E007000

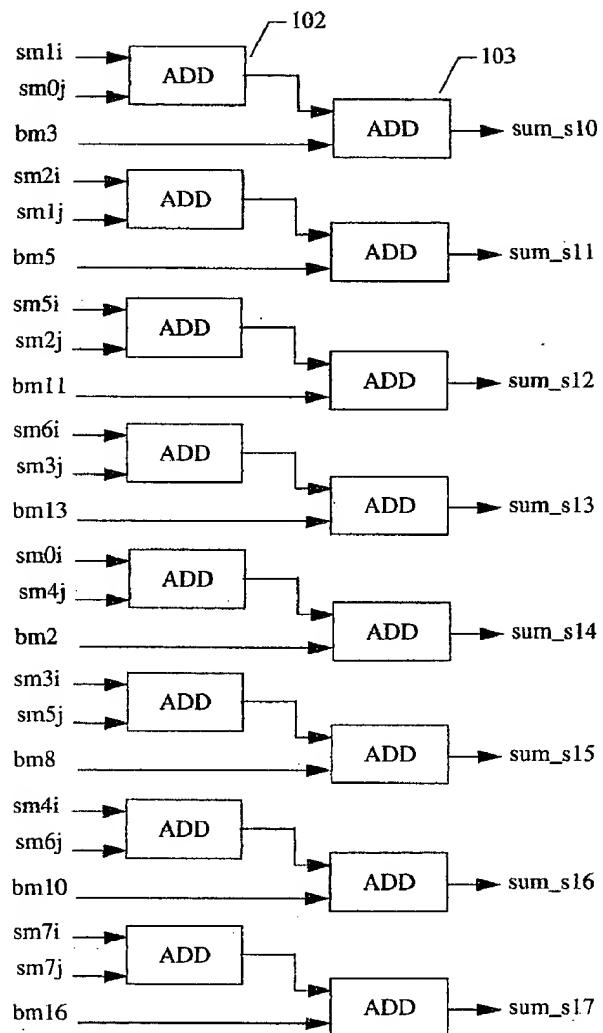


FIGURE 10b. LOG-MAP COMPUTING MODULE

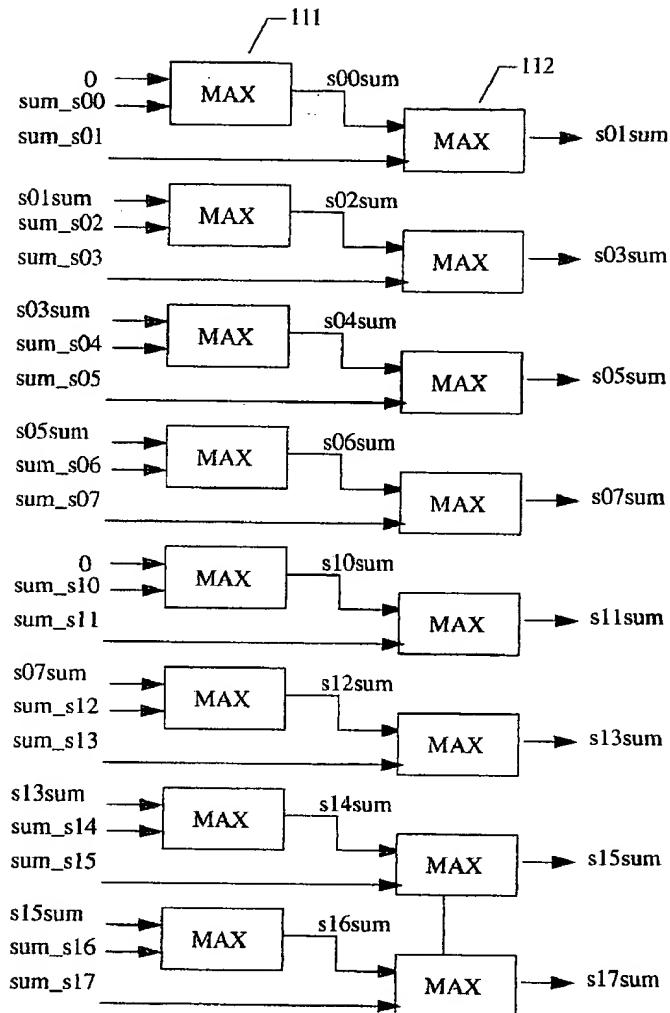


FIGURE 11. Computing Log-MAP for each state

09681093 - 010201

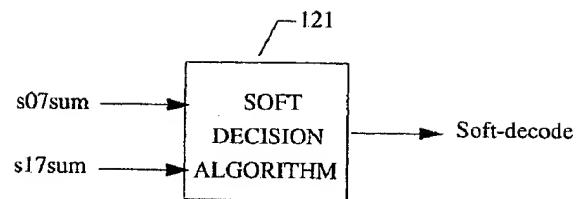


FIGURE 12. Soft Decode output

00634093-030204

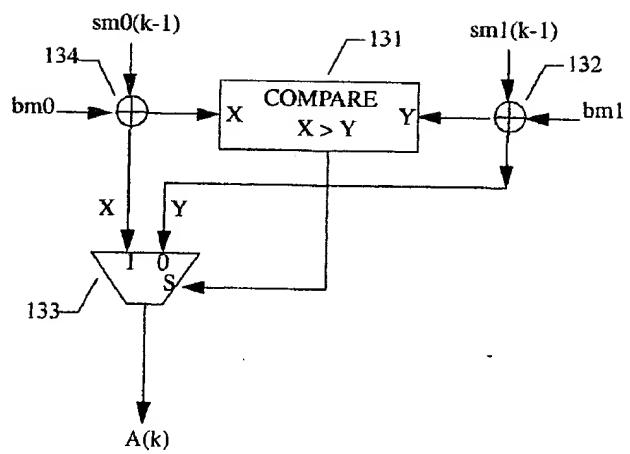


FIGURE 13. Computation of Forward Recursion of state-metric (ACS)

O G E N E R A L C O U R T

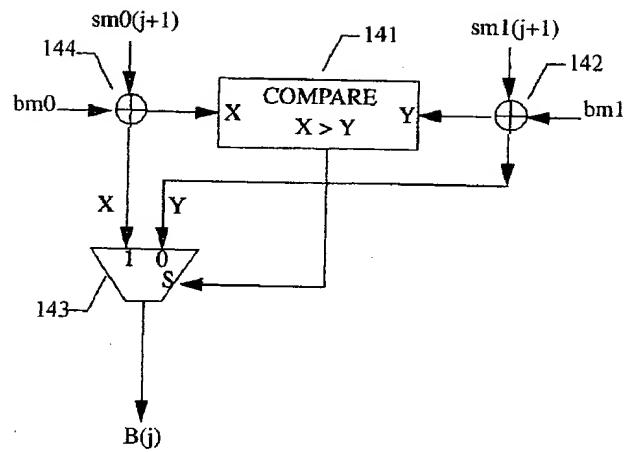


FIGURE 14. Computation of Backward Recursion of state-metric (ACS)

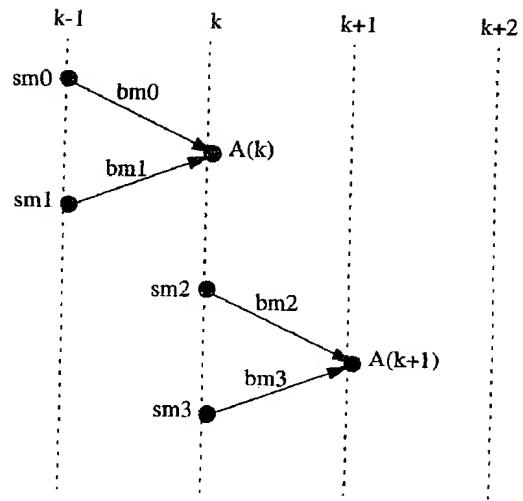


FIGURE 15. Forward computing of Trellis state transitions

09631093 - 64001

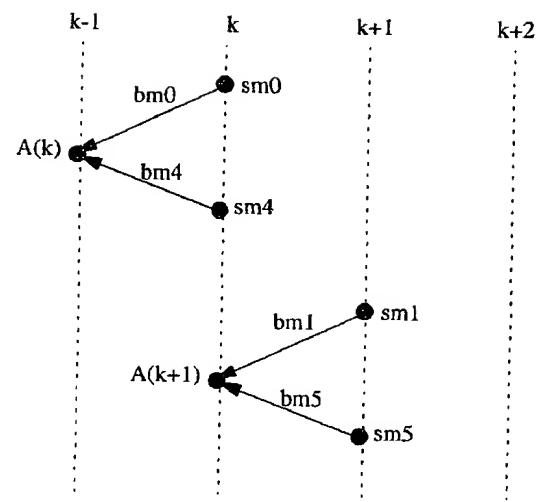


FIGURE 16. Backward computing of Trellis state transitions

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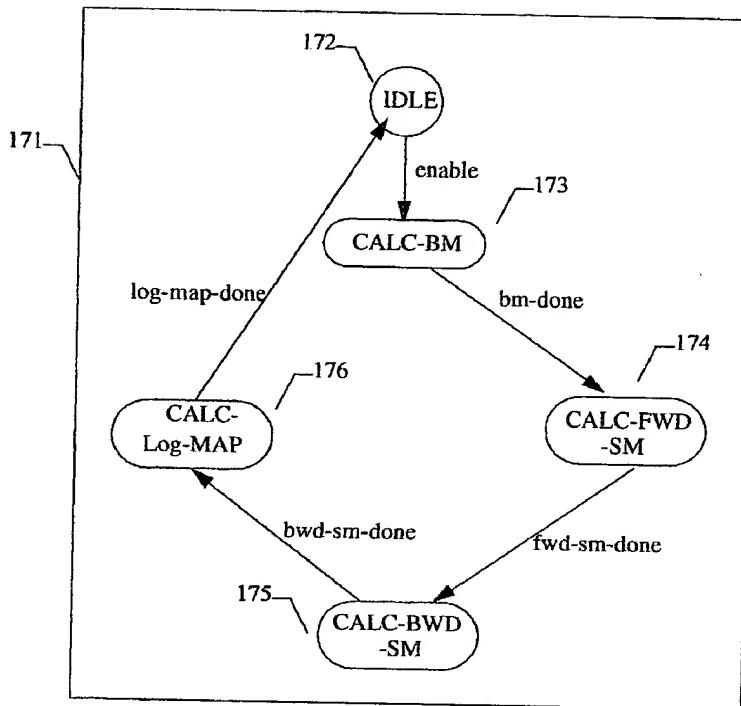


FIGURE 17. State machine operations of Log-MAP Decoder

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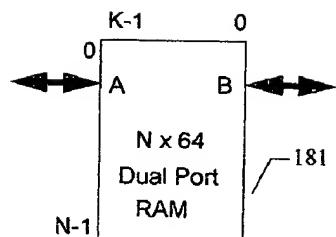


FIGURE 18. BM dual-port Memory Module

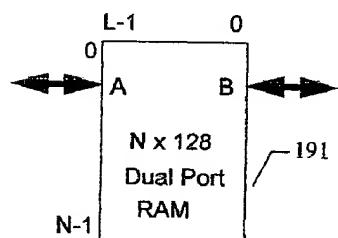


FIGURE 19. SM dual-port Memory Module

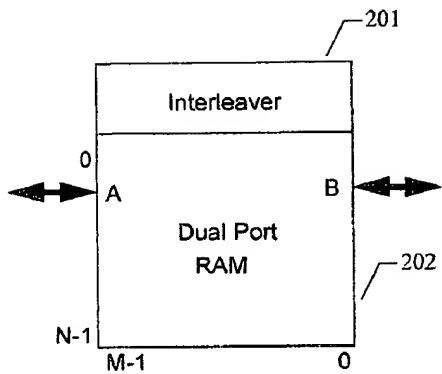


FIGURE 20. Interleaver RAM Memory Module

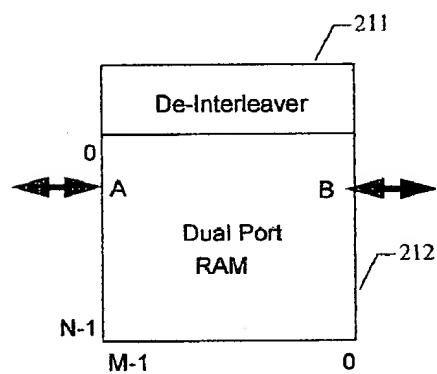


FIGURE 21. De-Interleaver RAM Memory Module

09531093 - 040264

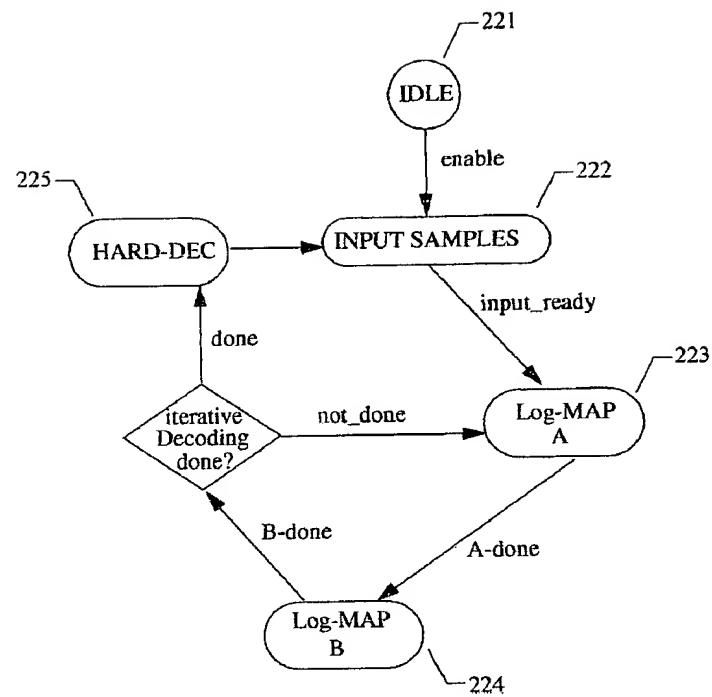


FIGURE 22. State machine operations of Turbo Decoder

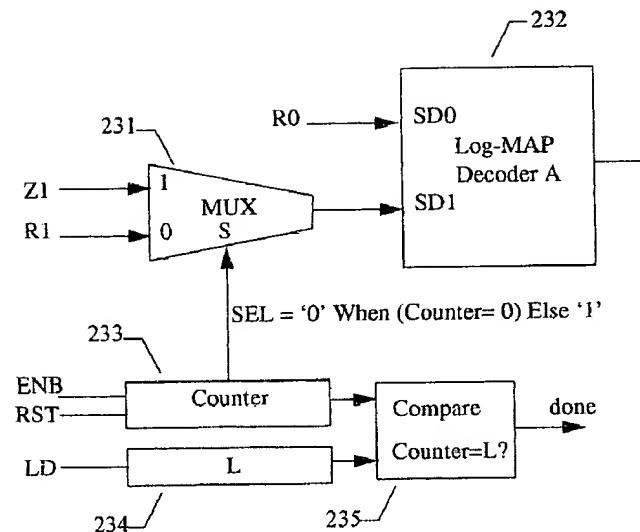


FIGURE 23. Iterative decoding feedback control Mux